ABSTRACT: In CMOS applications as device scaling, obeying Moore’s law reduces the active area of the devices to nearly atomic dimensions. The high-k dielectrics need to be used to prevent the tunneling effects which increase the leakage currents. In recent years, several emerging high-k materials have attracted enormous attention as potential candidates for electronic devices. Silicon dioxide (SiO₂) has been used as dielectric for more than 40 years because of its manufacturability and ability to deliver continued transistor performance improvements as it has been made ever thinner. Among the many potential high-k materials, LaAlO₃ has recently attracted much attention due to its many advantages such as high dielectric constant, high bandgap, and amorphous structure up to high temperature.

KEYWORDS: Tri State Inverter, CMOS, VLSI, Low Power, High-K.

INTRODUCTION

Over decades of incremental improvement to CMOS processing, the limitations of the SiO₂ gate dielectric layer have hung over the silicon industry as its single biggest technical challenge. To improve MOS transistor performance in the past, chip manufacturers have shrunk the thickness of the gate dielectric to as little as five atomic layers (1.2 nm). Although this has helped transistors reach new performance levels, it has also led to other problems such as increased leakage currents.

The requirements for high-k dielectric applications are:
1. High dielectric constant and large band gap.
2. High band offset with silicon.
3. Thermally and chemically stable in contact with semiconductor substrate.
4. Compatibility with gate electrode material.
5. Good reliability (no charge trapping, high breakdown voltage etc.)

This work overcomes some problems:
1. To reduce the leakage current.
2. Enhance the performance of a tri state inverter.

This work is based on six different dielectric materials (SiO₂, Si3N₄, Al₂O₃, Ta₂O₅, HfO₂, and LaAlO₃) and three different semiconductors (Ge, Si, and GaAs).

Firstly design the mathematical analysis of tri-state inverter to find out the length and width for different combination of material sand then study the properties of different materials i.e.
- Electron Mobility
- Hole Mobility
- Band gap (eV)
- Dielectrics constant
- Length (microns)

Hence find out which dielectric material is effective.

Comparison between Si and GaAs:
Both Gallium Arsenide (GaAs) and Silicon(Si) need the same lithographic process. But some of the advantages of Gallium Arsenide over Silicon are:
- The high speed electron mobility of gallium arsenide with respect to silicon.
- A semi-insulating substrate with consequent lowers parasitic.
- An improvement factor of 1.4 for carrier saturation velocity of GaAs over silicon.
- Better Opto-electrical properties.
- Less power dissipation than silicon and radiation hardness.

From the comparison of various physical and electronic properties of GaAs with those of Si the advantages of GaAs over Si can be readily ascertained.

<table>
<thead>
<tr>
<th>Properties</th>
<th>Ge</th>
<th>Si</th>
<th>GaAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>16.0</td>
<td>11.9</td>
<td>13.1</td>
</tr>
<tr>
<td>Intrinsic carrier conc. (cm-3)</td>
<td>2.4 x 10¹³</td>
<td>1.45 x 10¹⁰</td>
<td>1.79 x 10⁶</td>
</tr>
<tr>
<td>Intrinsic Debye Length(Microns)</td>
<td>0.68</td>
<td>24</td>
<td>2250</td>
</tr>
<tr>
<td>Mobility (cm²/V.s,electrons)</td>
<td>3900</td>
<td>1500</td>
<td>8500</td>
</tr>
<tr>
<td>Mobility (cm²/V.s, hole)</td>
<td>1900</td>
<td>450</td>
<td>400</td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>0.66</td>
<td>1.12</td>
<td>1.424</td>
</tr>
<tr>
<td>Intrinsic resistivity (ohm.cm)</td>
<td>47</td>
<td>2.3 x 10⁵</td>
<td>10⁸</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>72.60</td>
<td>28.09</td>
<td>144.63</td>
</tr>
<tr>
<td>Crystal structure</td>
<td>Diamond</td>
<td>diamond</td>
<td>zinc blende</td>
</tr>
<tr>
<td>Lattice constant</td>
<td>5.646</td>
<td>5.431</td>
<td>5.653</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>937</td>
<td>1415</td>
<td>1238</td>
</tr>
</tbody>
</table>

Table 1.1 Comparison of semiconductor Material

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant (K)</th>
<th>Band gap (eV)</th>
<th>CB Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>39</td>
<td>9</td>
<td>3.2</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7</td>
<td>5.3</td>
<td>2.4</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>9</td>
<td>6</td>
<td>2.8</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>22</td>
<td>4.4</td>
<td>0.35</td>
</tr>
<tr>
<td>HfO₂/ZrO₂</td>
<td>25</td>
<td>5.8</td>
<td>1.4</td>
</tr>
<tr>
<td>LaAlO₃</td>
<td>30</td>
<td>5.6</td>
<td>1.8</td>
</tr>
<tr>
<td>TiO₂</td>
<td>40</td>
<td>3.2</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1.2 Comparisons of Alternate High-K Values with SiO₂

2. LITERATURE REVIEW

The initial work and the interest in topic started from the paper published “Nano scale Tri Gate MOSFET For Ultra Low Power Applications Using High-K Dielectrics” by D...
The basic CMOS inverter is no more connected to the supply lines $V_{dd}$ and $V_{ss}$ directly. In contrast, pass n-MOS and pMOS devices are inserted to disconnect the inverter when the cell is disabled. We see that when $Enable=1$ the cell acts as a regular CMOS inverter, while when $Enable=0$ the output "floats" in an unpredictable voltage value, which tends to fluctuate at the switching of the input, mainly due to parasitic leakage and couplings.

There are three main sources for leakage current:
1. Source/drain junction leakage current.
2. Gate direct tunneling leakage.
3. Sub-threshold leakage through the Channel of an OFF transistor.

4. PROPOSED METHODOLOGY
The way in which this work is carried out is represented in a flow chart.

Fig: - 4.1 Flow Chart

5. CONCLUSION
In this paper, different dielectric materials are explored on tri state inverter. Different combination of the oxide and semiconductors are used. The structure will be drawn and simulated using microwind software. Number of different oxides likewise silicon dioxide, silicon Nitride, Aluminum oxide, Tantalum oxide, Hafnium Oxide, Lanthanum Oxide and three semiconductors are Gallium Arsenide, Silicon and Germanium are used. The mathematical analysis of the tri state inverter for the leakage current is required and then compare all the respective results for all the combinations of the oxide and semiconductor and conclude the results that which material having the minimum leakage current.

6. REFERENCES

### Table 3.1 Truth Table of Tri State Inverter

<table>
<thead>
<tr>
<th>In</th>
<th>En</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

3. TRI STATE INVERTER
The CMOS inverter design is consist of one p-channel MOS and one n-channel MOS transistors are used as switches. All the symbols produced the value logic ‘0’ and logic ‘1’. However, if several inverters share the same node, such as bus structure conflicts will rise. In order to avoid multiple access at the same time, specific circuits called Tristate inverters are used, featuring the possibility to remain in a ‘high impedance’ state when access is not required. The Tristate inverter symbol consists of the logic inverter and an enable control circuit. The output remains in ‘high impedance’ (Logic symbol 'X') as long as the enable $En$ is set to level '0'.

Nirmal, P Vijay Kumar and Doreen Joy, Proceeding of IEEE 5th International Nanoelectronics Conferences (INCE). In this paper they tried to show that CMOS Technology has seen excellent high speed performance achieved through improved design, use of high quality and processing innovations over past decades. Silicon dioxide gate dielectric is replaced with various high-k dielectric materials and the simulations have carried out. It is observed that the leakage of the device decreased by about 54%. Further this concept was carried forward by D Nirmal and P Vijay Kumar and they published a paper “Impact of Gate Engineering on Double Gate MOSFETs Using High-k Dielectrics” IEEE 2011. In this paper, it is clearly analyzed the influence of gate engineering on ID-VGS characteristics, trans-conductance of dual material doubled gate MOSFET for different high-k dielectrics using ISE TCAD. The gate engineered devices show an increase of drain Current by about 5% in sub threshold region and 3% increase in transconductance region.

J. Conde, A. Cerdeira, M. Pavanello, V. Kilelytska and D. Flandre, “3D Simulation of Triple-Gate MOSFETs” 27th international conference on microelectronics (miel 010), nis, serbia, 16-19 may, 2010.

This paper present a new approach of analyzing 3D structure for Triple-Gate MOSFETs with three different mesh regions, one at the top and two in the sidewalls of the fin, which allows the consideration of different carrier mobility at each region due to the crystalline orientation and technological processing. A procedure for the extraction of the mobility parameters in each region is developed. Validation of the proposed structure was made for a FinFET arrays with fixed channel length and different fin widths, obtaining a very good coincidence between experimental and simulated characteristics.

Francisco J. Garcia Ruiz, Isabel Maria Tienda-Luna, Andres Godoy “Equivalent Oxide Thickness of Trigate SOI MOSFETs With High-K Insulators” IEEE transactions on electron devices, vol. 56, no. 11, November 2009.

This paper demonstrates that the typical expression of equivalent oxide thickness (EOT) for planar devices with high-K gate insulators becomes useless for non-planar ones such as triple-gate (tri-gate) silicon-on-insulator MOSFETs.


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